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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/678,419	10/03/2003	Neil McLellan	50626.59	1002

7590 10/18/2004  
KEATING & BENNETT LLP  
Suite 312  
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EXAMINER
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TRAN, MAI HUONG C

ART UNIT	PAPER NUMBER
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2818

DATE MAILED: 10/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No. 10/678,419	Applicant(s) MCLELLAN ET AL.	
	Examiner Mai-Huong Tran	Art Unit 2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 03 October 2003.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-18 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 03 October 2003 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |   |  |
|---|--|
| <p>1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)</p> <p>2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)</p> <p>3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br/>Paper No(s)/Mail Date <u>10/3/03</u></p> | <p>4) <input type="checkbox"/> Interview Summary (PTO-413)<br/>Paper No(s)/Mail Date. _____</p> <p>5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)</p> <p>6) <input type="checkbox"/> Other: _____</p> |
|---|--|

## **DETAILED ACTION**

### **Drawings**

The drawings are objected to for the following reasons.

Figure 1 is not designated by a legend such as "Prior Art". The Legend is necessary in order to clarify what applicant's invention is (see MPEP § 608.02g).

Reference sign 140 on page 4, [0020] of the specification is not included in the drawings (see 37 CFR § 1.84p). Correction is required.

### **Claim Rejections - 35 U.S.C. § 102**

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-6 are rejected under 35 U. S. C. § 102 (b) as being anticipated by U.S. Patent No. 6,069,023 To Bernier et al. (hereinafter Bernier).

Regarding to claim 1, figure 4 of Bernier discloses an integrated circuit package comprising a substrate 242 having first and second surfaces and a plurality of conductive traces (fig. 4) therebetween; a semiconductor die flip-chip 248 mounted to the first surface of the substrate 242 and electrically connected to ones of the conductive traces

(fig. 4); an intermetallic (col. 15, lines 35-36) heat spreader 246 fixed to a back side of the semiconductor die 248; and a plurality of contact balls (fig. 4) disposed on the second surface of the substrate 242, in the form of a ball grid array, ones of the contact balls of the ball grid array being electrically connected with ones of the conductive traces (col. 8, lines 54-62, and fig. 4).

Regarding to claim 2, Bernier discloses the integrated circuit package wherein the semiconductor die 248 is flip-chip mounted to the first surface of the substrate and electrically connected to ones of the conductive traces via a plurality of solder ball connectors (col. 8, lines 54-62, and fig. 4).

Regarding to claim 3, Bernier discloses the integrated circuit package further comprising an underfill material surrounding the solder ball connectors (col. 8, lines 40-62, and figs. 3, 4).

Regarding to claim 4, Bernier discloses the integrated circuit package wherein the solder ball connectors are comprised of eutectic solder (col. 7, lines 30-41, col. 9, lines 3-4, and figs. 2, 5).

Regarding to claim 5, Bernier discloses the integrated circuit package wherein the intermetallic heat spreader is fixed to the backside of the semiconductor die by a thermally conductive adhesive (col. 6, lines 46-48, col. 8, lines 57-59).

Regarding to claim 6, Bernier discloses the integrated circuit package wherein the intermetallic heat spreader is fixed to the backside of the semiconductor die by a thermally conductive epoxy (col. 8, lines 57-59).

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1 and 7-8 are rejected under 35 U. S. C. § 102 (e) as being anticipated by U.S. Patent No. 6,583,513 to Utagikar et al. (hereinafter Utagikar).

Regarding to claim 1, figures 2 and 3 of Utagikar discloses an integrated circuit package comprising a substrate 120 having first and second surfaces and a plurality of conductive traces 160 therebetween; a semiconductor die flip-chip 110 mounted to the

first surface of the substrate 120 and electrically connected to ones of the conductive traces 160; an intermetallic heat spreader 144 fixed to a back side of the semiconductor die 110; and a plurality of contact balls 150 disposed on the second surface of the substrate 120, in the form of a ball grid array, ones of the contact balls 150 of the ball grid array being electrically connected with ones of the conductive traces 160 (col. 5, lines 64-67, col. 6, lines 1-31).

Regarding to claim 7, Utagikar discloses the integrated circuit package wherein the intermetallic heat spreader 144 comprises a first portion fixed to the backside of the semiconductor die 110 and a plurality of sidewalls in contact with the substrate 120 (col. 6, lines 22-31, and fig. 3).

Regarding to claim 8, Utagikar discloses the integrated circuit package wherein the sidewalls are fixed to the substrate 120 (fig. 3).

### **Claim Rejections - 35 U.S.C. § 103**

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention

was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 9 and 10 are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 6,583,513 to Utagikar et al. in view of the remark.

Regarding to claim 9, Utagikar discloses the claimed invention except for the integrated circuit package wherein the heat spreader is fixed to a plurality of intermediate sidewalls at a plurality of sites, each of the intermediate sidewalls being fixed to the substrate. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the heat spreader that is fixed to a plurality of intermediate sidewalls at a plurality of sites, since it has been held that modifying the structure of the device, where needed, involves only routine skill in the art.

Regarding to claim 10, Utagikar discloses the intermediate sidewalls comprise an intermetallic material (col. 6, lines 29-31).

Claims 11, 12, 16 and 17 are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 6,069,023 to Bernier et al. in view of the remark.

Regarding to claims 11, 12, 16 and 17, Bernier discloses an integrated circuit package comprising a substrate 242 having first and second surfaces and a plurality of

conductive traces (fig. 4) therebetween; a semiconductor die flip-chip 248 mounted to the first surface of the substrate 242 and electrically connected to ones of the conductive traces (fig. 4); a heat spreader 246 having a coefficient of thermal expansion of Cu about 17 ppm/°C or of Al about 23.4 ppm/°C, fixed to a back side of the semiconductor die 248; and a plurality of contact balls (fig. 4) disposed on the second surface of the substrate 242, in the form of a ball grid array, ones of the contact balls of the ball grid array being electrically connected with ones of the conductive traces (col. 8, lines 54-62, and fig. 4).

Bernier does not disclose the intermetallic heat spreader having a coefficient of thermal expansion in the range of about 18 ppm/°C to about 26 ppm/°C.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the heat spreader of Bernier comprising an intermetallic compound (col. 15, lines 34-36) having a coefficient of thermal expansion in the range of about 18 ppm/°C to about 26 ppm/°C in order to increase thermal conduction and to also reduce delamination problems (col. 2, line 67, col. 3, line 1), since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.



Claims 13 is rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 6,069,023 to Bernier et al. in view of Chen et al. (hereinafter Chen) (Pub. No. US 2003/0150595).

Regarding to claim 13, Bernier discloses the claimed invention except for the integrated circuit package wherein intermetallic compound comprises  $\text{CuAl}_3$ .

However, Chen teaches the intermetallic compound comprises  $\text{CuAl}$  (page 1, [0012]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the intermetallic compound comprising  $\text{CuAl}$ , as taught by Chen in order to accomplish the external configuration of various heat sinks through direct compression casting for dissipating high heat sources in a central process unit of a computer (page 1, [0002]).

Claims 14 and 18 are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 6,069,023 to Bernier et al. in view of Alcoe et al. (US 6,570,259) (hereinafter Alcoe).

Regarding to claims 14 and 18, Bernier discloses the claimed invention except for the intermetallic compound has a modulus of elasticity of at least the modulus of elasticity of the semiconductor die.

However, Alcoe discloses a semiconductor chip package, wherein the intermetallic compound 46 has a modulus of elasticity of at least the modulus of elasticity of the semiconductor die (col. 7, lines 4-12).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the intermetallic compound having a modulus of elasticity of at least the modulus of elasticity of the semiconductor die, as taught by Alcoe in order to provide a package for the semiconductor chip that minimizes stresses and strains that arise from differential thermal expansion (col. 5, lines 18-21).

Claim 15 is rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 6,069,023 to Bernier et al. in view of Shaw et al. (U.S. Patent No. 5,330,701) (hereinafter Shaw).

Regarding to claim 15, Bernier discloses the claimed invention except for the integrated circuit package wherein the intermetallic compound comprises NiAl. Shaw discloses the intermetallic compound comprises NiAl (col. 1, lines 15-29, lines 49-55). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the intermetallic compound comprises NiAl as taught by Shaw in order to have the attractive characteristics of low density, high strength, good corrosion and oxidation resistance, and relatively low cost. The specific combination of low density


and high strength makes these materials excellent candidates for uses in which high strength is required in conjunction with minimum weight (col. 1, lines 20-32).

### Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mai-Huong Tran whose telephone number is (571)272-1796. The examiner can normally be reached on 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571)272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

  
10/4/04

  
Mai-Huong Tran  
Examiner  
Art Unit 2818